Q-Pix: Status & Prospects of a Pixelated Readout Concept for large LArTPCs

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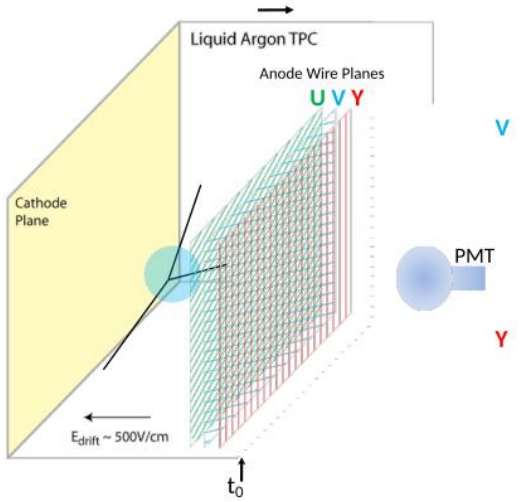
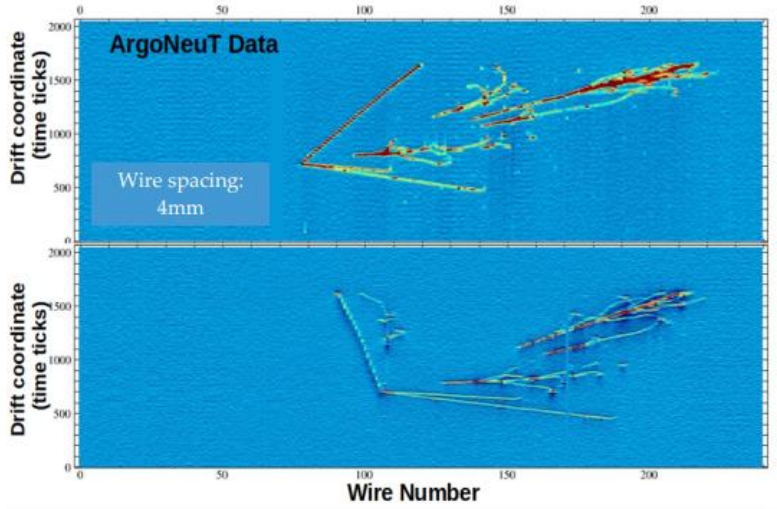
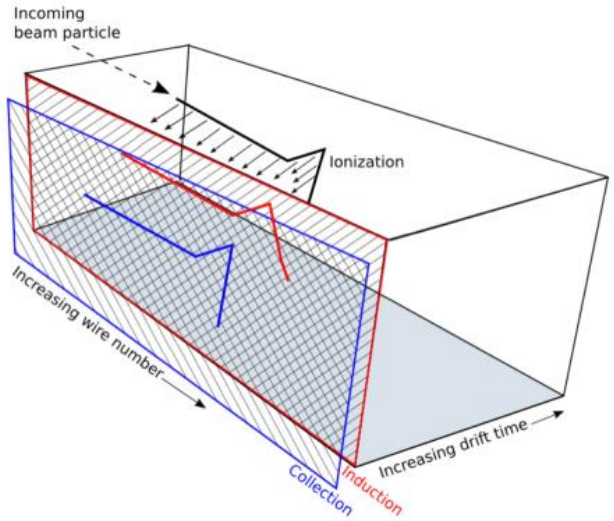
Introduction: LAr Time Projection Chambers

- Primary ionized particles drift in electric field.
- Prompt light emission by ions gives a reference T0.
- Induced current on the anode wires
- Initial ionization position is reconstructed from (usually) wire signals: time gives coordinate along E and wires position give coordinates in anode plane.





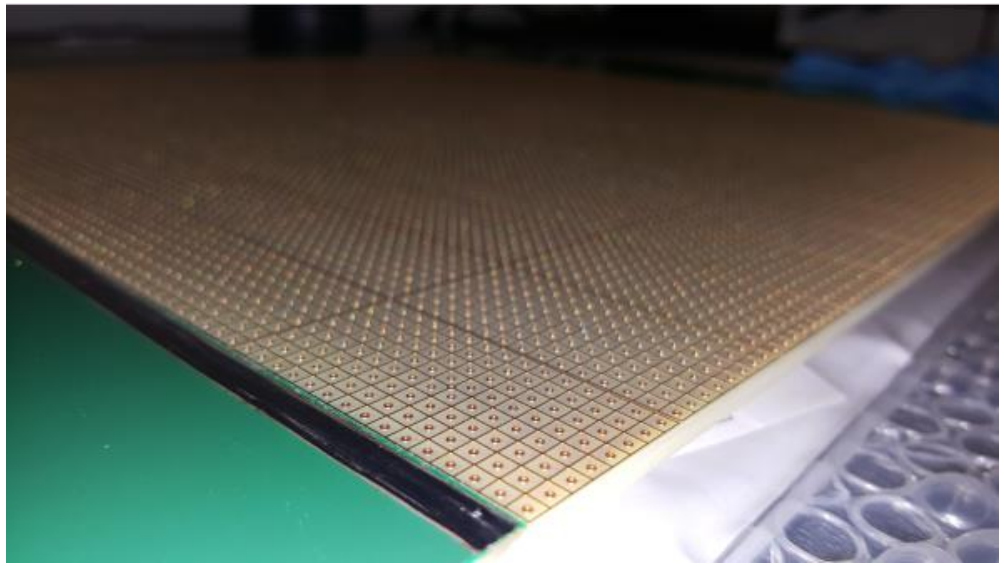


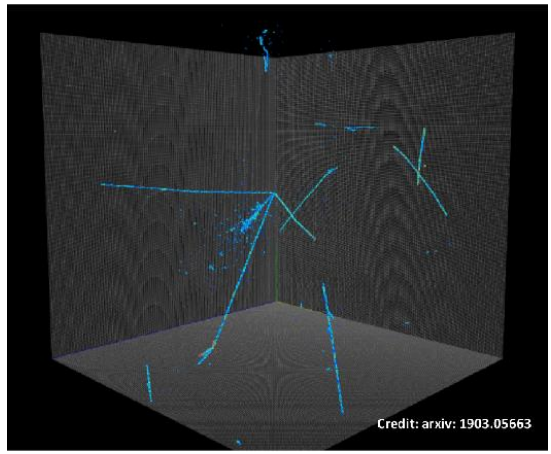
<u>Challenges for wire-plane readout</u>:

- Pathologies associated with charge deposited along the wires.
- Ambiguity in reconstruction of 3D images.
- Complex topologies can be difficult to reconstruct.

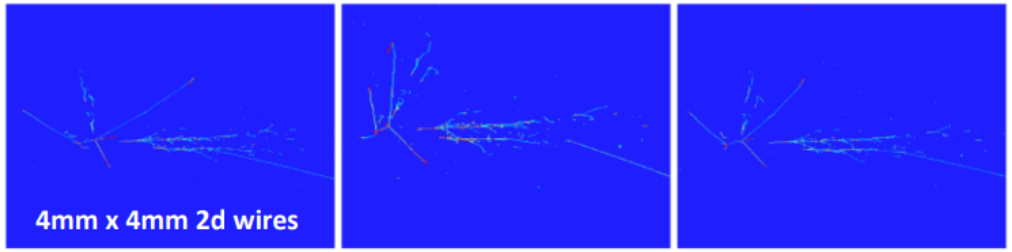
Pixelated Readout?

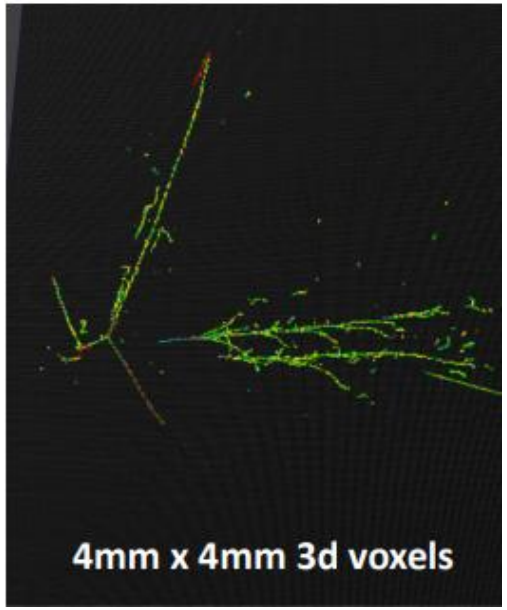
- Switching from wires to pixels avoid ambiguities in track reconstruction…
- …but very challenging.
  - e.g., 10kTon DUNE module:
    - O(1.5M) wires
    - O(130M) pixels
  - Large pixel count – potential issues w/ heat dissipation, data volume, cabling, ...
- … introducing Q-Pix.





JINST 15 P04009 gives an example of comparing 2D vs. 3D readout reconstruction performance.



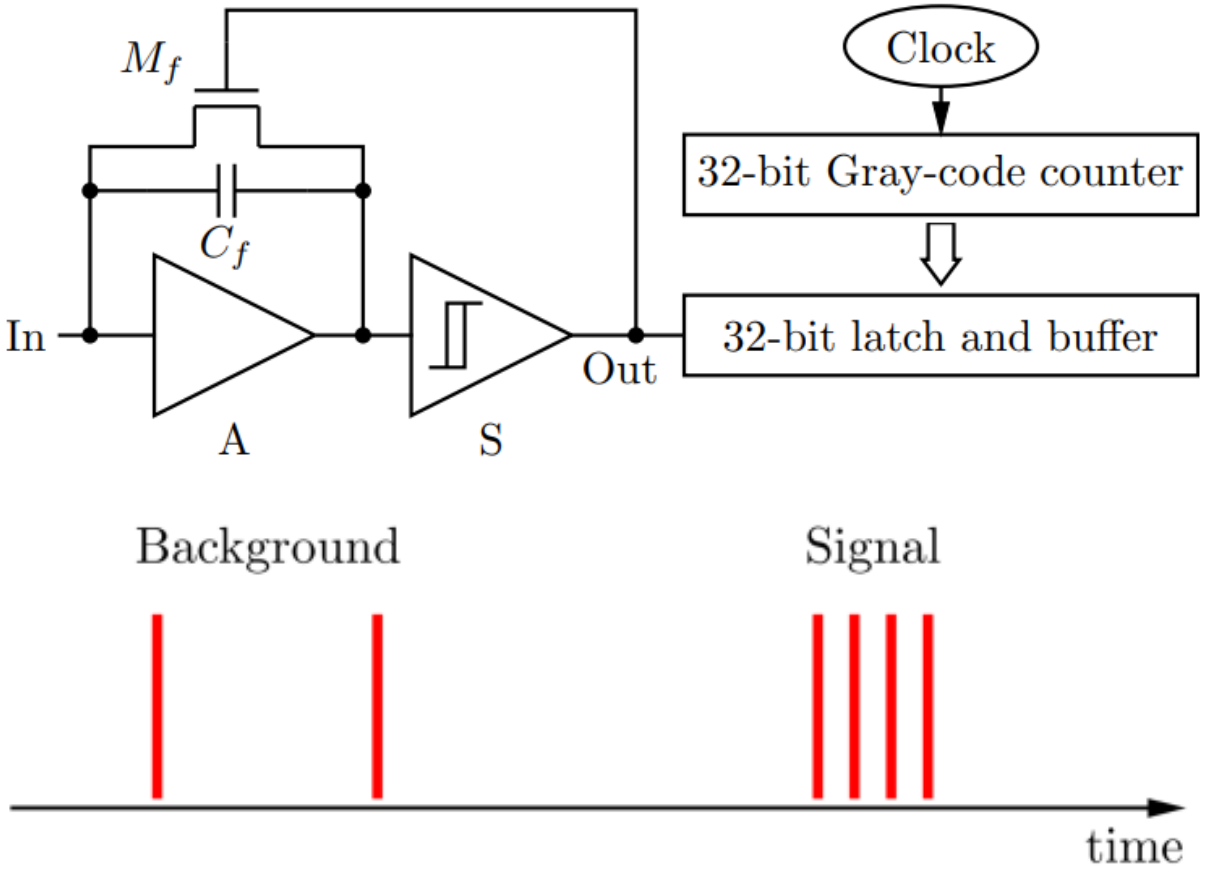


Q-Pix Concept*

*from D. Nygren, Y. Mei [arXiv:1809.10213]

- Most of the time, there is no signal, but must be ready to record at any moment.
- A time-to-charge solution can provide a solution to high channel counts, immense data rates, high power.
- Core pixel block is the charge-integrate-reset (CIR) circuit, shown to the right.
  - Input charge integration stage.
  - Compare integrated charge to a threshold.
  - When threshold is reached, the reset switch shorts out the feedback capacitor and drains its charge.
    - This reset pulse is timestamped.
    - These timestamps allow reconstruction of the incident signal.

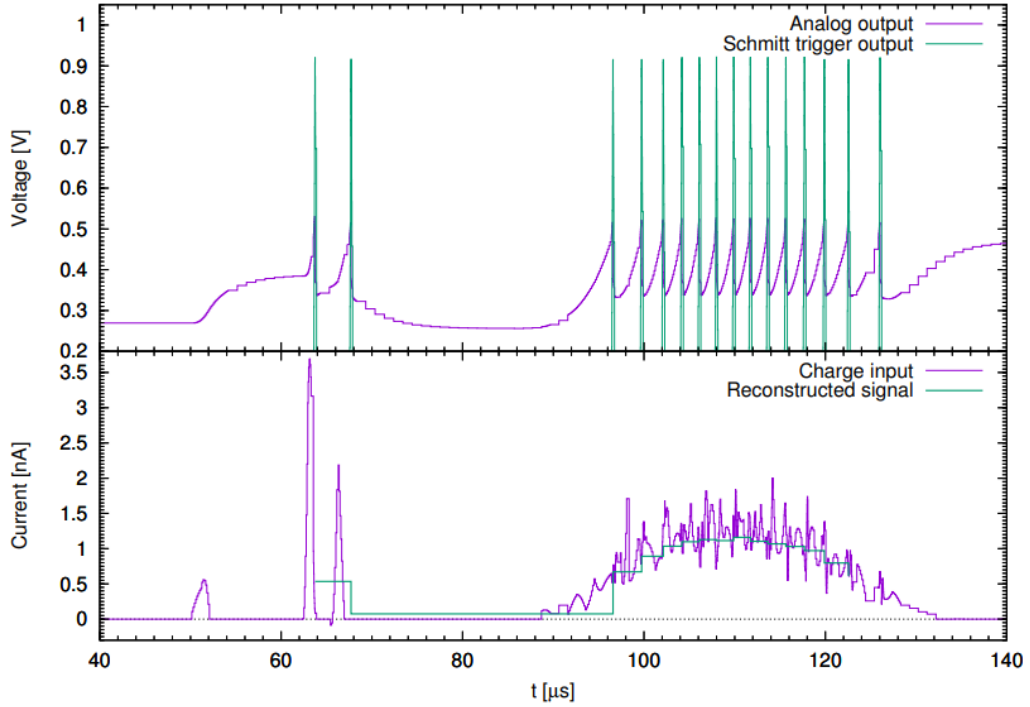
**This also allows for



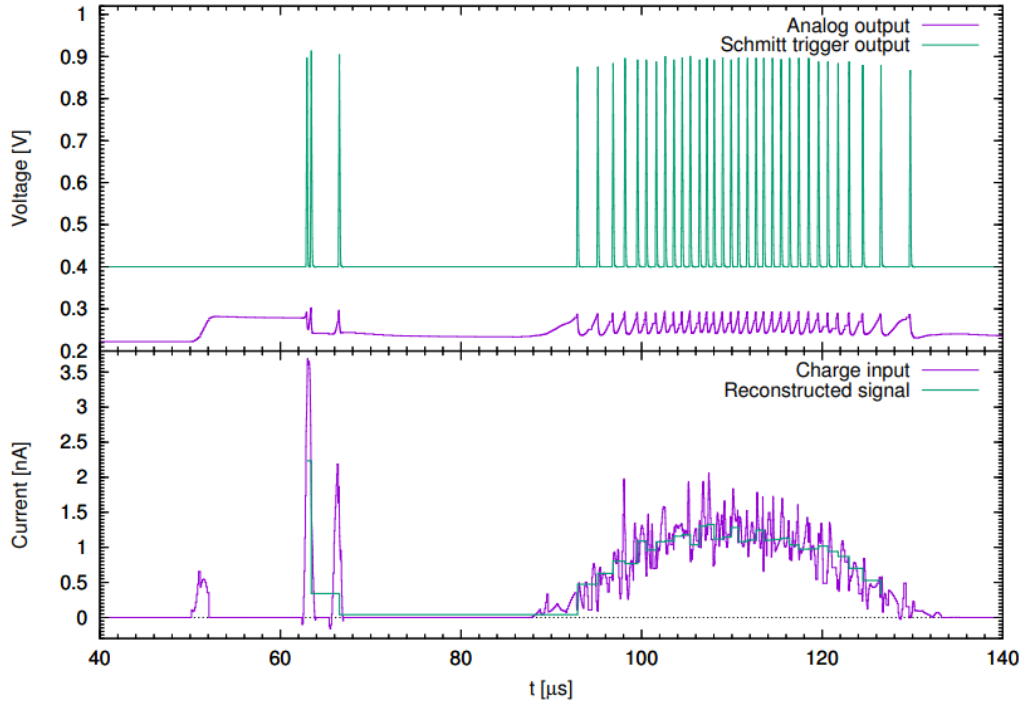
Example Reconstructions

- Thresholds on integrated charge can determine ability to reconstruct original waveform.

Example w/ 1.0 fC Threshold



Example w/ 0.3 fC Threshold

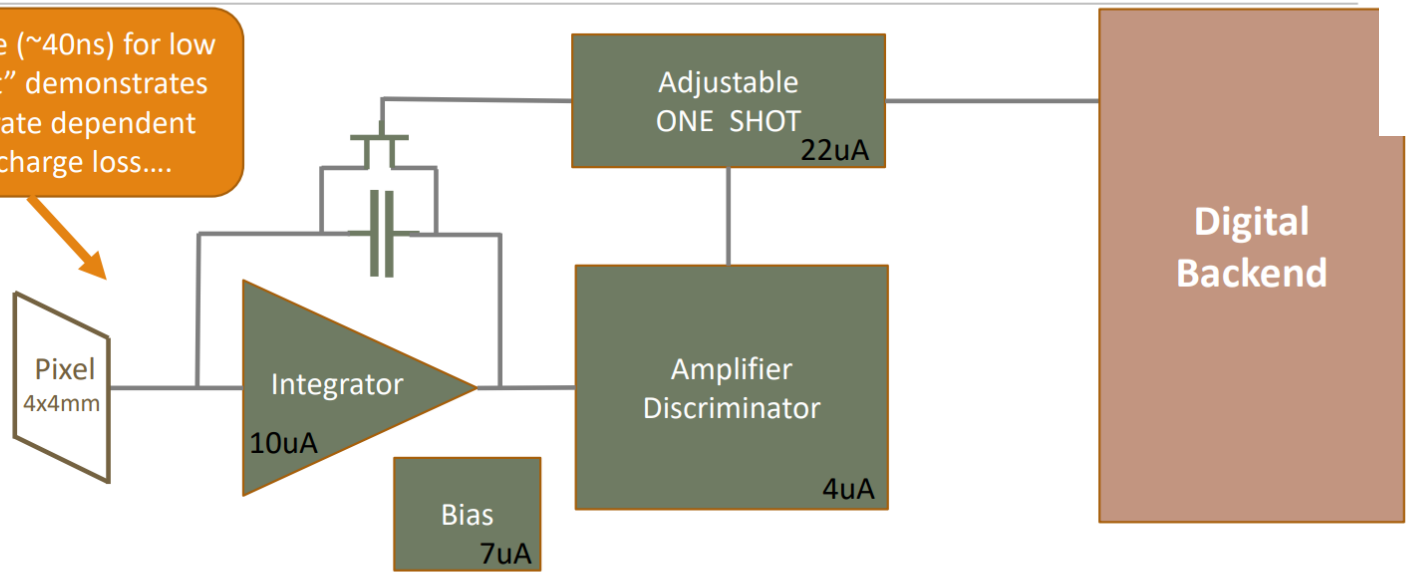


Initial CIR DESIGN

- **<TO BE UPDATED>**

Q-Pix analog front end - First attempt

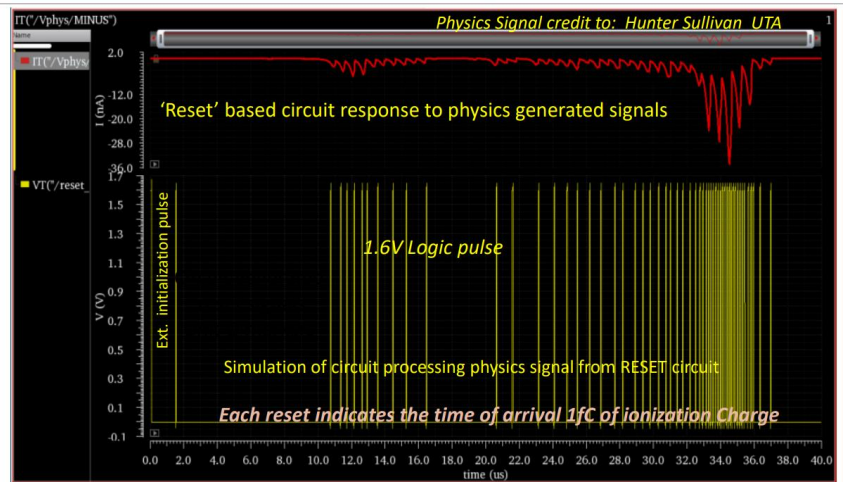
The finite time (~40ns) for low power "reset" demonstrates instigates a rate dependent ionization charge loss....



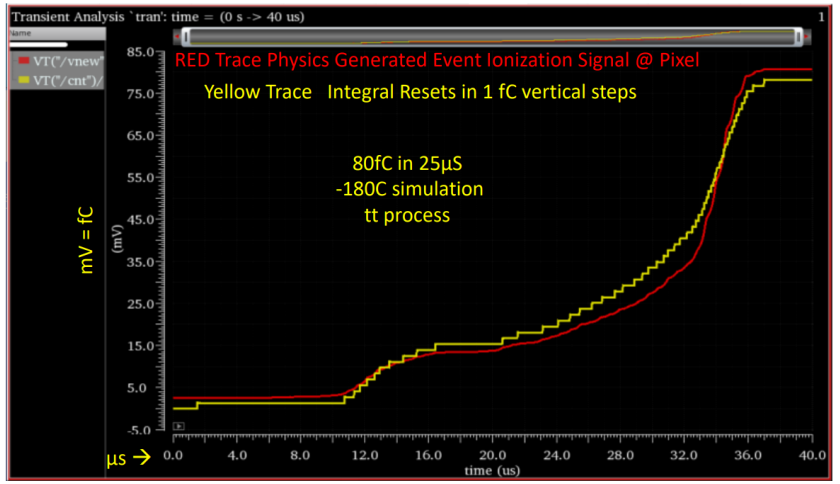
Schematic Level design in 180nm Silicon
Proven @LAr temperatures -186C°
re: LArASIC (BNL) and LArPix (LBNL)

Single (FE only) Channel POWER/ch	
Present FE Design	34µW
Projected final prototype FE	**25µW**

Simulation results with physics generated signal

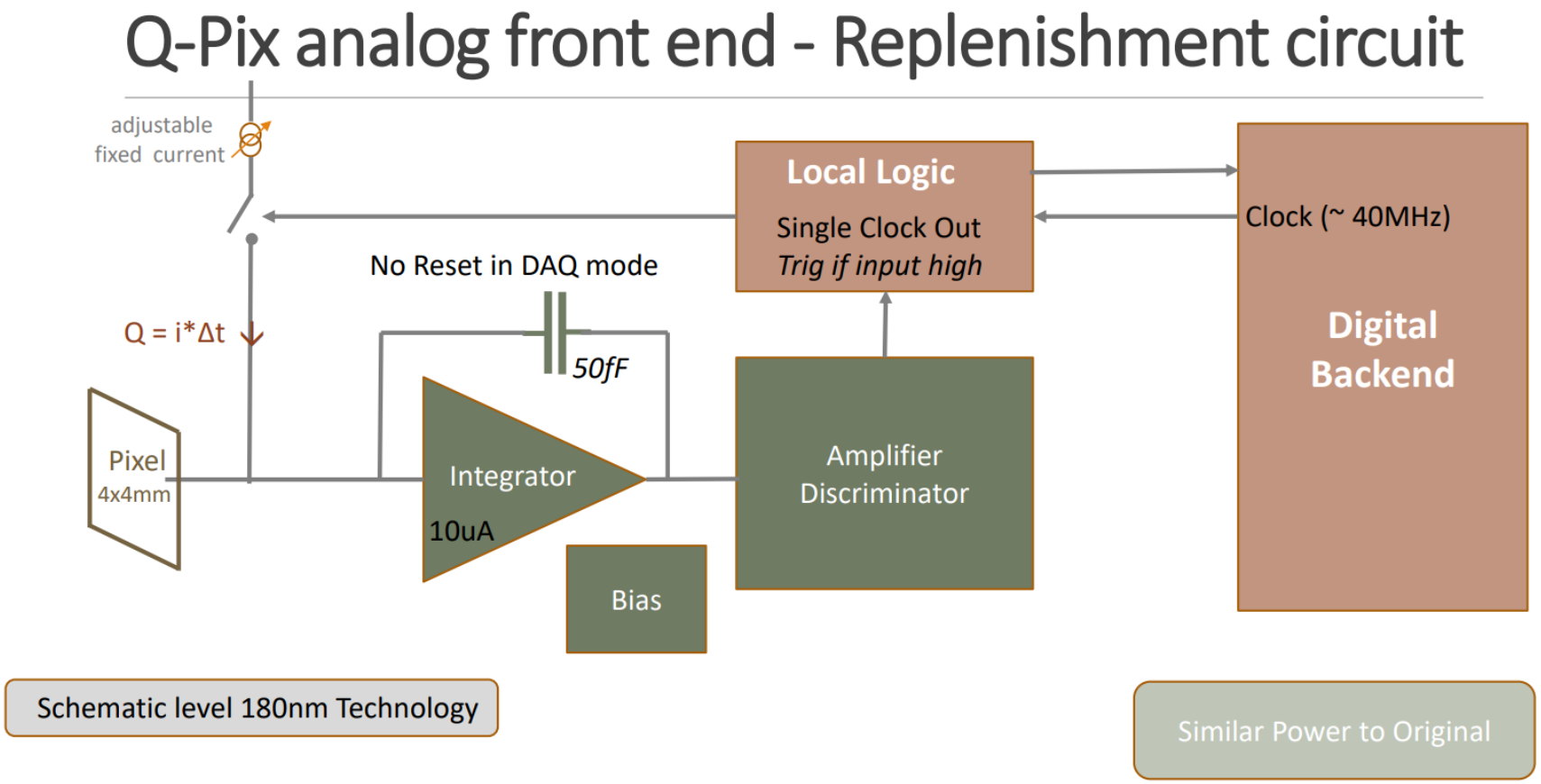


Reconstruction of the signal using reset time marking

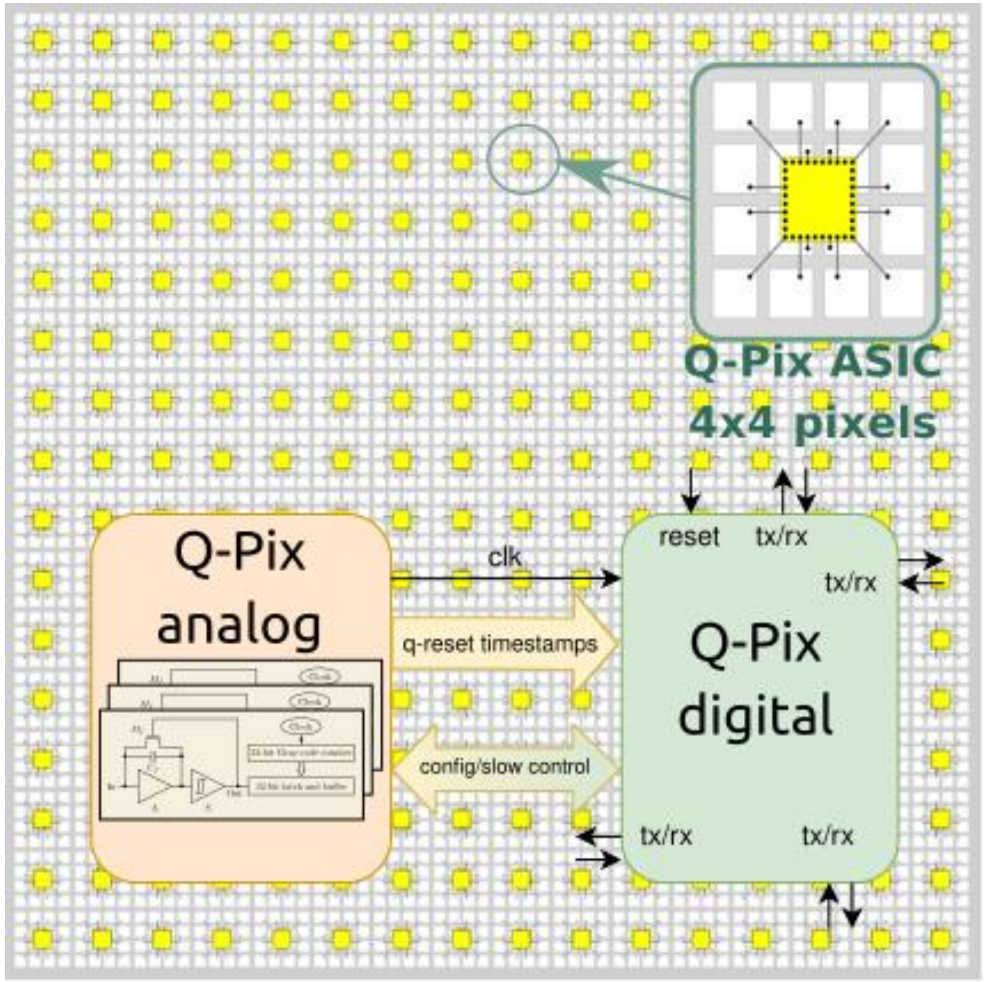


Replenishment Alternative

- ***<TO BE UPDATED>***



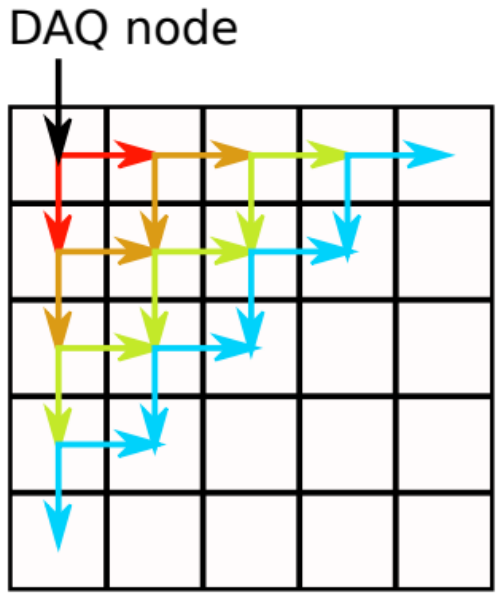
The Q-Pix ASIC



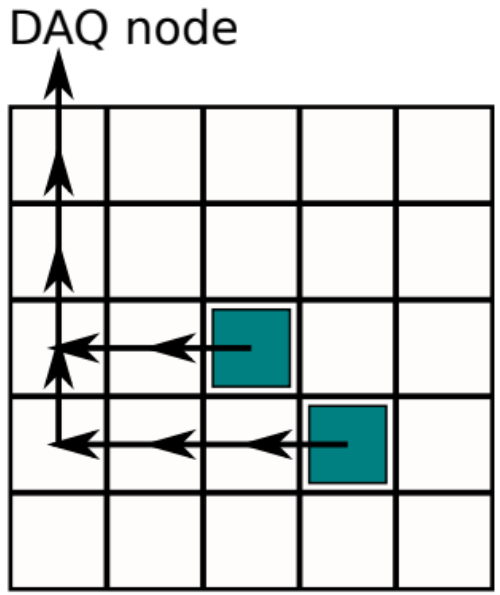
- Pixels implemented on PCB.
- Each pixel connects to a Q-Pix CIR circuit.
- 16-32 CIRs per ASIC.
- Multiple ASICs connected into a tile.
- ASICs form a (reconfigurable) network to communicate hits to one or more data collection nodes.
- External requests from a data collection node trigger readout of a full tile at some fixed interval.

Data Path

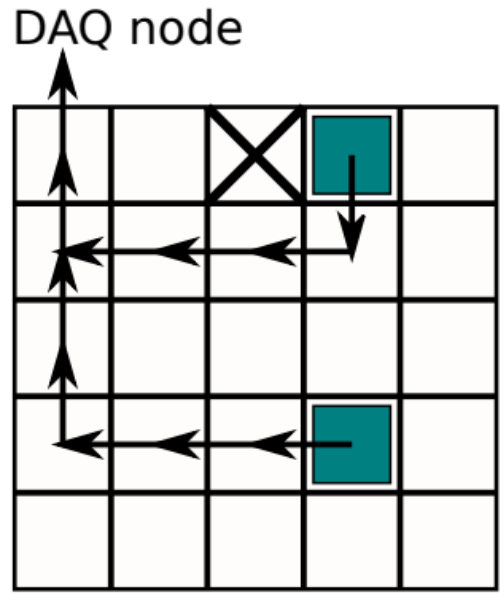
- ASICs have own clocks.
- *Asynchronous* serial connection between ASICs.
  - UART
  - Penn "Endeavor" protocol (Morse-code)



registers request/ interrogation



data path

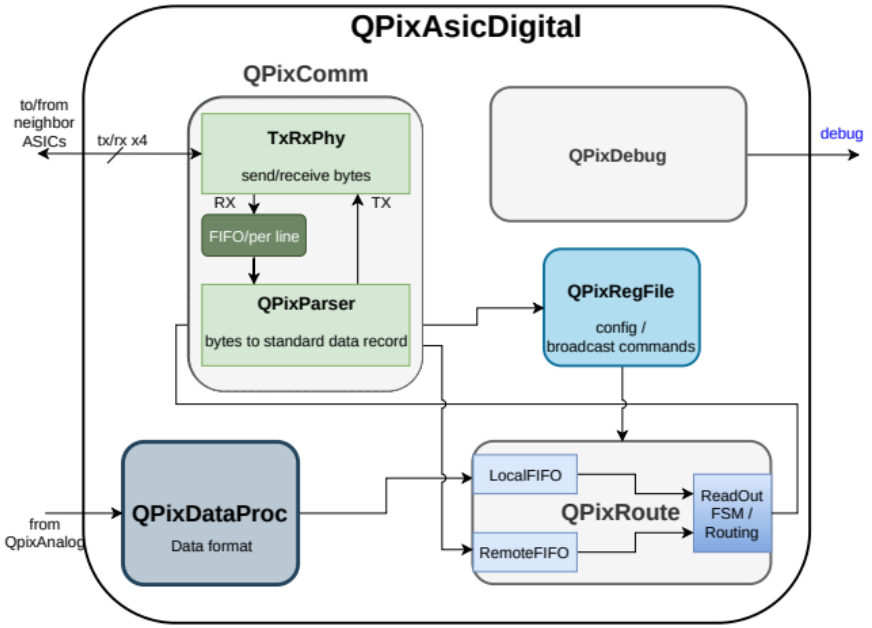


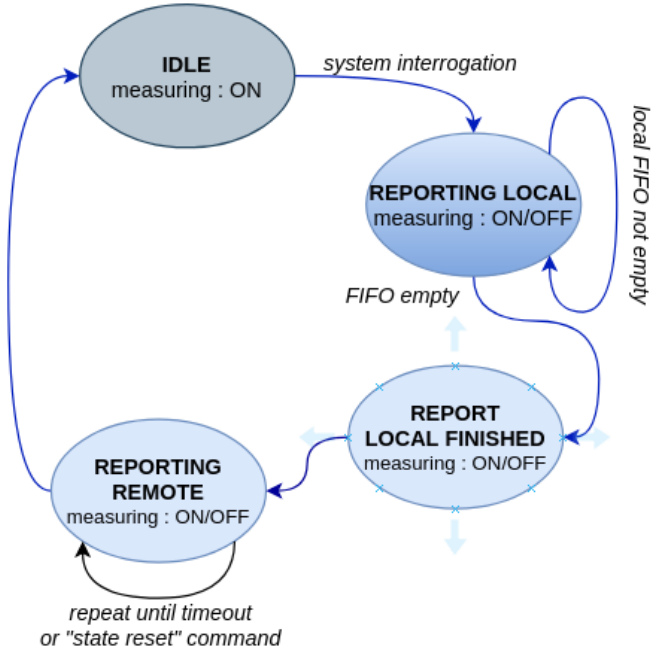
data path w/ broken ASIC

- Register read/writes & readout requests are broadcasted to all neighbor ASICs (by default 4x connections).
- A request has it's ID not to be processed twice and avoid data looping.
- ASIC coordinates serve as an address for targeting reads/writes.
- Data paths can be reprogrammed through register control.

Digital Design Overview

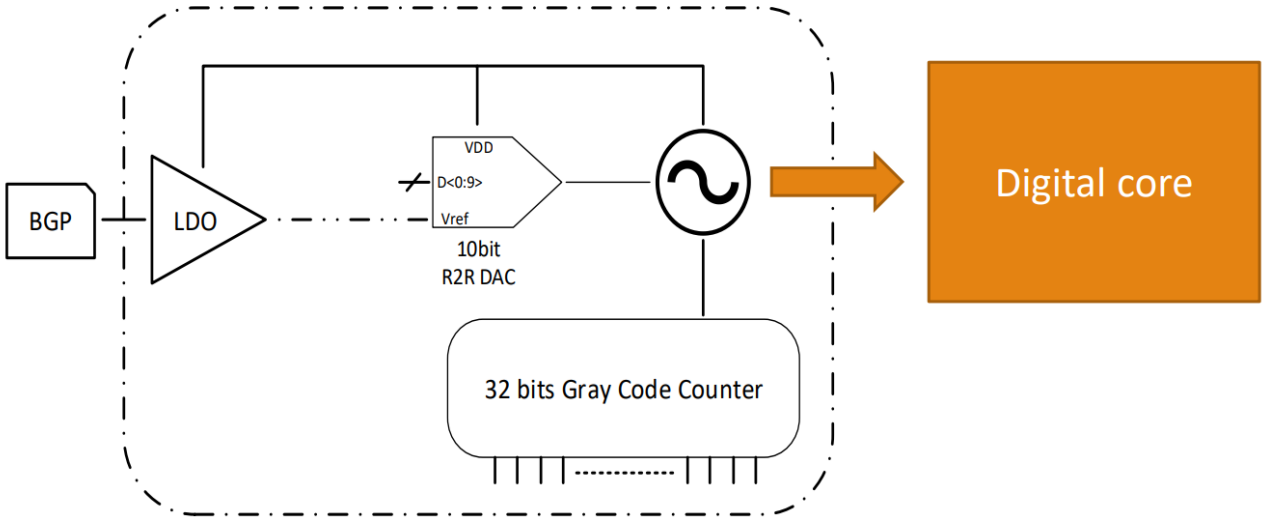
- **IDLE state:**
  - CIR timestamps are stored locally into a FIFO. Digital comms are quiet.
  - System interrogation is received from a neighbor (or DAQ node), move to next state.
- **REPORTING LOCAL state:**
  - Send local FIFO hits back to where the interrogation request came from.
  - Can continue to record hits (or not).
- **REPORTING LOCAL FINISHED state:**
  - Can continue to record hits (or not).
- **REPORTING REMOTE state:**
  - Pass along hits from neighbors back to where interrogation request came from until a timeout.
  - Can continue to record hits (or not).

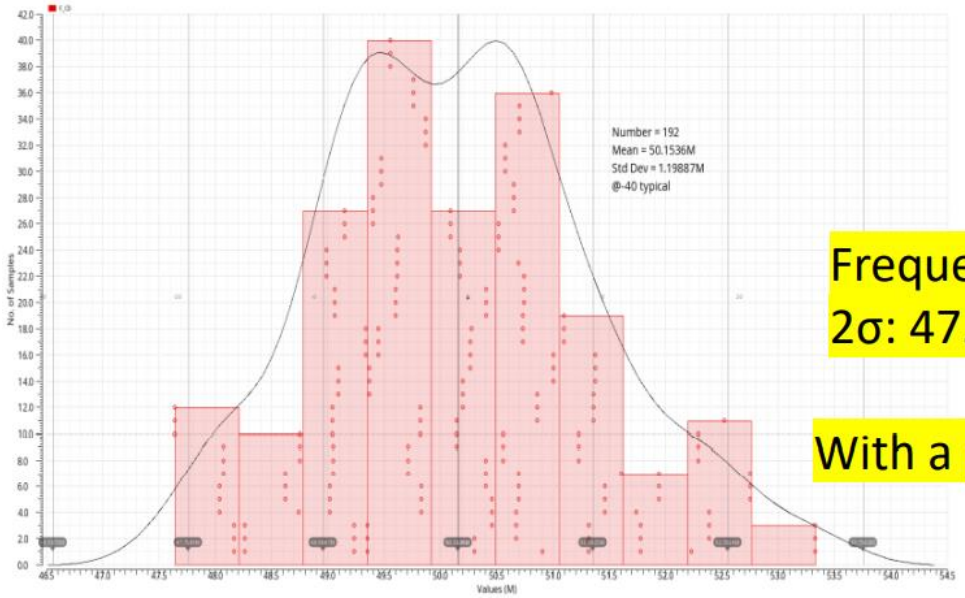


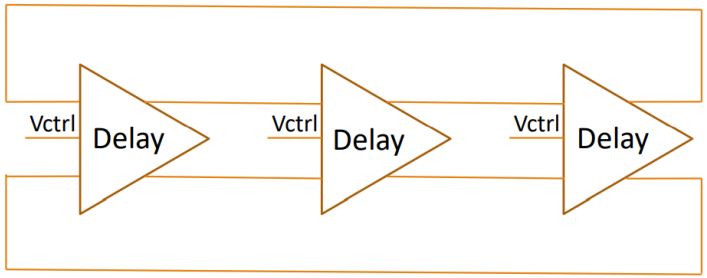


Free Running Clock

- Aim for ~20-50 MHz for timestamping.
- Spread in frequencies among devices determined largely by requirements of async communications protocols.





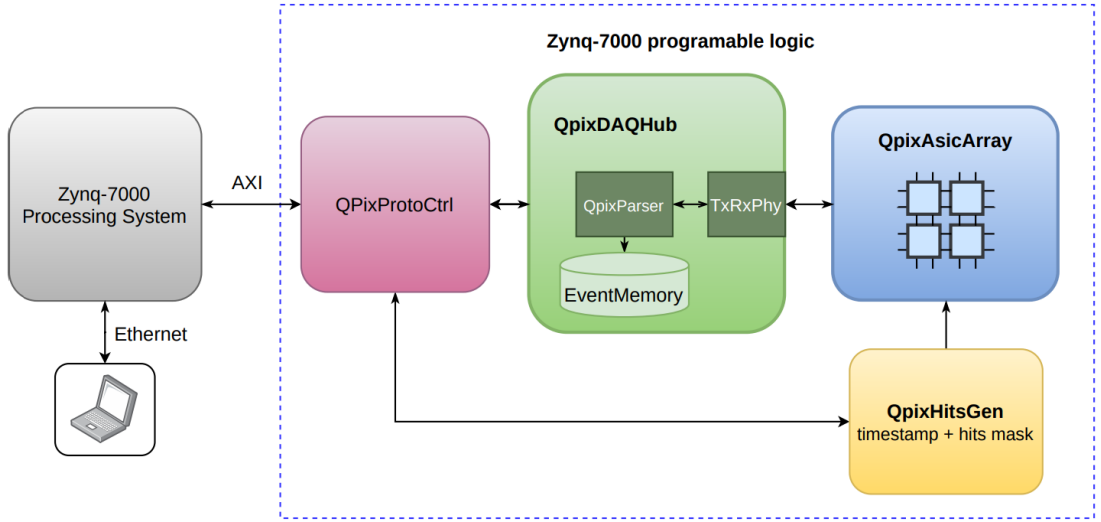


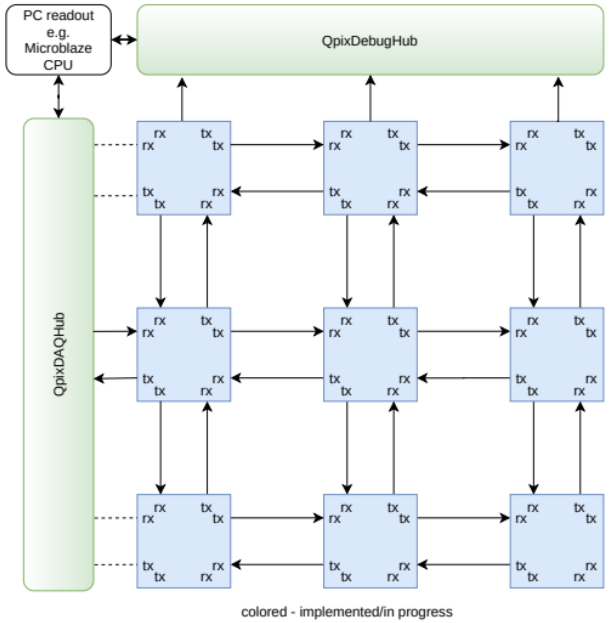
Frequency monte carlo simulation
2σ: 47.76M ~52.56M @-40 typical
Approx +/- 4.5%
With a power of 0.35mW @ 50MHz

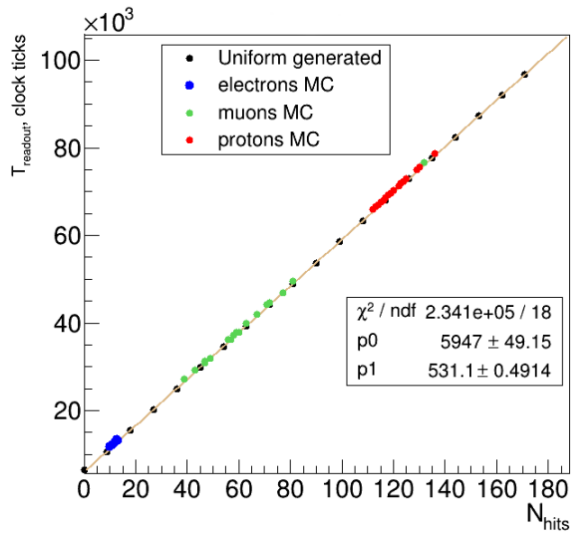
- Initial design:
  - 3-stage ring oscillator.
  - Differential structure.
  - R2R DAC and power supply.

Digital Prototyping

- Prototypes implemented in Xilinx Zynq SoCs:
  - Digital design is implemented within FPGA fabric.
  - 3x3 mini-tile of "ASICs" in the same FPGA.
  - Simulation samples for electrons, muons, protons fed into FPGA.
    - Readout chain is run, can measure how readout times scale with number of hits.
    - Can study performance with memory depths, data transfer protocols, …
- Basic functionality verified, but all on the same clock domain.
- Now designing a new low-power FPGA-based digital tile to demonstrate the final asynchronous version of system.







Readout time in number of the clock cycles when using UART protocol.

Summary and Outlook

- Q-Pix is a novel architecture that can allow for pixelated readout of LAr TPCs.
  - Key features:
    - Charge-integrate-reset (or replenish) circuit.
    - Independent ASICs arranged into a reconfigurable network on a tile.
    - Individual clocks to avoid clock distribution.
- Plans toward tapeout and ASIC:
  - First front-end analog CIR designs to tape out late 2021.
  - Initially planning to support CIR designs with FPGA to fully validate logic.
  - Move toward independent digital ASIC (or eventually fully mixed analog/digital).